REMARKS/ARGUMENTS

Claims 1 and 2 are currently pending in the application and have been amended. Claims 3-6 are withdrawn from consideration.

The Examiner objected to claims 1 and 2 because of informalities. Applicant has amended claims 1 and 2 to correct for such informalities.

Applicant has amended claims 1 and 2 to more clearly define the invention. Applicant notes the amendments to claims 1 and 2 were not required based on the references cited by the Examiner.

The Examiner rejected claims 1-2 under 35 USC § 103(a) as being unpatentable over Shinohara (U.S. Publication No. 2003/0189656). Applicant traverses this rejection and requests reconsideration of the application.

Official Notice

The Examiner took Official Notice with respect to the use of CCD shift registers for a column line of an image sensor. The Examiner stated "that both the concepts and advantages of using CCD shift registers for a column line of an image sensor are well known and expected in the art." Section 2144.03 of the Manual of Patent Examining Procedure (MPEP) states "assertions of technical facts in the areas of esoteric technology or *specific knowledge of the prior art* must always be supported by citation to some reference work recognized as standard in the pertinent art" (emphasis added). Applicant notes the Examiner did not support the Official Notice with a citation to some reference work recognized as a standard in the pertinent art. Applicant respectfully requests the Examiner provide such citation or documentary evidence in the next Office Action if this rejection is maintained.

Section 2144.03 of the MPEP further states that if Official Notice is taken, "the basis for such reasoning must be set forth explicitly. The Examiner must provide specific factual findings predicated on sound technical and scientific reasoning to support his or her conclusion of common knowledge." Applicant notes the Examiner did not provide any reasonings or specific factual findings regarding the actual claim limitation in claim 1. Specifically, the Examiner did not provide any reasoning or specific factual findings for having "at least two charge-coupled devices adjacent the first photosensitive region." Applicant respectfully requests the Examiner provide such reasoning or specific factual findings in the next Office Action if this rejection is maintained.

103(a) Rejection

The Manual of Patent Examining Procedure states the following in Section 2143:

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Applicant submits Shinohara does not render Applicant's claims obvious because the Shinohara does not meet the three basic criteria. The argument below, however, will focus on the third criterion.

Claim 1 recites "at least two charge-coupled devices adjacent the first photosensitive region." The Examiner argues Figure 2 in Shinohara teaches at least two charge-coupled devices adjacent the first photosensitive region. Applicant respectfully disagrees with the Examiner. Figure 2 shows Shinohara's invention connected to a column line (30). A column output line does not teach or suggest a charge-coupled device. Moreover, Applicant is claiming at least two charge-coupled devices adjacent one photosensitive region. Nothing found in Shinohara teaches or suggests this aspect of the invention.

Claim 1 further recites "a first transfer gate associated with the first photosensitive region that selectively passes charge to the at least two charge-coupled devices at first and second voltage levels." The Examiner argues "22-24, 26, 28 makes [*sic*] up one transfer gate and shows the charges being transferred to a column line 30 and two levels being used to transfer two depth regions TxB, TxG and is shown to be transferring selectively at different times." Applicant respectfully submits Shinohara does not teach elements 22-24, 26, and 28 form one transfer gate. Shinohara expressly states in paragraph [0032]:

> Reference numeral 19 denotes a transfer MOS transistor used to transfer a signal charge of the photodiode 16; 20, a transfer MOS transistor used to transfer a signal charge of the photodiode 17; 21, a transfer MOS transistor used to transfer a signal charge of the photodiode 18; and 22, a transfer gate of the transfer MOS transistor 19, which corresponds to the transfer gate 13 in FIG. 1, and receives transfer signal TxR. Reference numeral 23 denotes a transfer gate of the transfer MOS transistor 20, which corresponds to the transfer gate 14 in FIG. 1, and receives transfer signal TxG. Reference numeral 24 denotes a transfer gate of the transfer MOS transistor 21, which corresponds to the transfer gate 15 in FIG. 1, and receives transfer signal TxB. (emphasis added)

Clearly, Shinohara teaches elements 22, 23, and 24 are separate and distinct transfer gates that each receive a particular transfer signal and perform distinct transfer functions. As shown in Figure 2, transfer gate 22 receives the transfer signal TxR. Shinohara states in paragraph [0032] that element 22 corresponds to the transfer gate 13 shown in Figure 1. Transfer gate 13 is described as a transfer gate that transfers a signal charge accumulated on the signal charge accumulation portion 7 to the floating diffusion 10 (paragraph [0029]).

Transfer gate 23 receives the transfer signal TxG (see Figure 2). Shinohara states element 23 corresponds to the transfer gate 14 shown in Figure 1 (paragraph [0032]). Transfer gate 14 is described as a transfer gate that transfers a signal charge accumulated on the signal charge accumulation portion 8 to the floating diffusion 11. (paragraph [0029]).

And finally, transfer gate 24 receives the transfer signal TxB (see Figure 2). Shinohara states in paragraph [0032] that element 24 corresponds to the transfer gate 15 shown in figure 1. Transfer gate 15 is described as a transfer gate that transfers a signal charge accumulated on the signal charge accumulation portion 9 to the floating diffusion 12 (paragraph [0029]). Thus, elements 22, 23, and 24 are separate and distinct transfer gates that each receive a particular transfer signal and perform distinct transfer functions.

With respect to elements 26 and 28, Shinohara states in paragraph [0032]:

> Reference numeral 26 denotes an amplification MOS transistor, the gate of which is connected to the FD 25. Reference numeral 27 denotes a reset MOS transistor used to reset the FD 25; 28, a selection MOS transistor used to select an output from the amplification MOS transistor; 29, a line which serves as both a reset power supply and a power supply for the amplification transistor 26; 30, an output line to

> which the amplified signal is output; and 31, a gate line of the reset MOS transistor 27, which receives reset signal RES. Reference numeral 32 denotes a gate line of the selection MOS transistor 28, which receives select signal SEL. (emphasis added)

Again, Shinohara teaches elements 26 and 28 are separate and distinct transistors that perform different functions. Element 26 is an amplification MOS transistor that has its gate connected to the floating diffusion (25). Element 28 is a selection MOS transistor that selects an output from the amplification MOS transistor and whose gate receives a select signal SEL.

Moreover, nothing found in Shinohara teaches or suggests selectively passing charge at first and second voltage levels. The transfer signals TxG, TxB, and TxR are illustrated in Figures 3 and 4. In these figures, all three transfer signals appear to have the same voltage levels. Additionally, the transfer signals TxG, TxB, and TxR are discussed in paragraphs [0034] through [0037]. The description states that when the transistors are of an n-type, the MOS transistors 19, 20, 21 are on when TxR, TxG, TxB, respectively, (i.e., the gate potentials) are at a High (H) level and off when the gate potentials are at a Low (L) level (paragraph [0034]). But Shinohara does not describe the actual voltage levels that represent H and L. Shinohara also does not disclose turning on the MOS transistors at two different voltage levels.

And finally, claim 1 recites "the at least first and second photosensitive regions are doped so that charge is collected and stored in two separate depth regions of the photosensitive regions." The Examiner argues Shinohara teaches this aspect of the claimed invention in paragraphs [0047] through [0054] and in Figure 7. Applicant respectfully disagrees with the examiner. Shinohara does not store the charges at different depths of the photosensitive regions. The charges generating in the photoelectric conversion regions 33, 34, 35, 36 (see Figures 5 and 7) accumulate at respective signal charge accumulation portions 37, 38, 39, 40 (see paragraph [0041]). The generated charges migrate to the signal charge accumulation portions 37, 38, 39, 40 because the accumulation portions 37, 38, 39, 40 have higher impurity concentrations than the photoelectric conversion portions 33, 34, 35, 36 (see paragraph [0041]). The higher impurity concentrations draw the charges to the

accumulation portions 37, 38, 39, 40. Thus, Shinohara teaches storing the generated charges at the accumulation portions 37, 38, 39, 40, and, as shown in Figures 5 and 7, the accumulation portions 37, 38, 39, 40 are all located at the same depth within pixels A and B.

Additionally, the fact that the charges are stored at the accumulation portions 37, 38, 39, 40 supports Applicant's arugments regarding the voltage levels of the transfer signals TxR, TxG, TxB. The three transfer signals TxR, TxG, TxB can use the same High (H) voltage level to transfer signals out of the photoelectric conversion regions 33, 34, 35, 36 because the charges are stored at the same depth within the pixels. Thus, while photoelectric conversion portion 33 is located at a deeper depth within pixel A than photoelectric conversion region 34, a higher voltage level is not needed to transfer charge out of photoelectric conversion region 33. The same voltage level can be used to transfer charge from photoelectric conversion portions 33, 34 because both of the accumulation portions 37, 38 are located at the same depth level within pixel A.

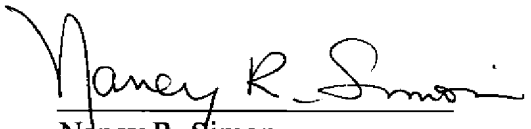
In conclusion, Shinohara does not teach or suggest all of the claim limitations in Applicant's independent claim 1. Shinohara does not disclose or suggest "at least two charge-coupled devices adjacent the first photosensitive region." Shinohara does not teach or suggest "a first transfer gate associated with the first photosensitive region that selectively passes charge to the at least two charge-coupled devices at first and second voltage levels." And finally, Shinohara does not disclose or suggest "the at least first and second photosensitive regions are doped so that charge is collected and stored in two separate depth regions of the photosensitive regions." Therefore, for at least the following reasons, independent claim 1 is not obvious in view of Shinohara.

"If an independent claim is not rendered obvious by prior art, then any claim depending from the independent claim is not obvious." In re Fine, 5 USPQ2d 1596 (Fed. Cir. 1988) (see also M.P.E.P. § 2143.03). Claim 2 depends from independent claim 1. Becuase independent claim 1 is not obvious in view of Shinohara, dependent claim 2 is also not obvious in view of Shinohara.

In view of the foregoing it is respectfully submitted that the claims in their present form are in condition for allowance and such action is respectfully requested.

The Commissioner is hereby authorized to charge any fees in connection with this communication to Eastman Kodak Company, Deposit Account No. 05-0225.

Respectfully submitted,



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If the Examiner is unable to reach the Applicant(s) Attorney at the telephone number provided, the Examiner is requested to communicate with Eastman Kodak Company Patent Operations at (585) 477-4656.